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McClure et al.

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(54) **PROTOCOL ADAPTER FOR PASSING DIAGNOSTIC MESSAGES BETWEEN A HOST COMPUTER AND VEHICLE NETWORKS OPERATING IN J1939 OR J1708 PROTOCOL**

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This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

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(60) Provisional application No. 60/126,588, filed on Mar. 26, 1999.

(51) **Int. Cl.**

G06F 13/12	(2006.01)
G06F 3/00	(2006.01)
G06F 15/173	(2006.01)

(52) **U.S. Cl.** **710/16**; 710/73; 710/74; 701/24; 701/29; 701/31; 701/33; 701/35; 701/36; 701/53

(58) **Field of Classification Search** 340/431, 340/933; 710/72–74

See application file for complete search history.

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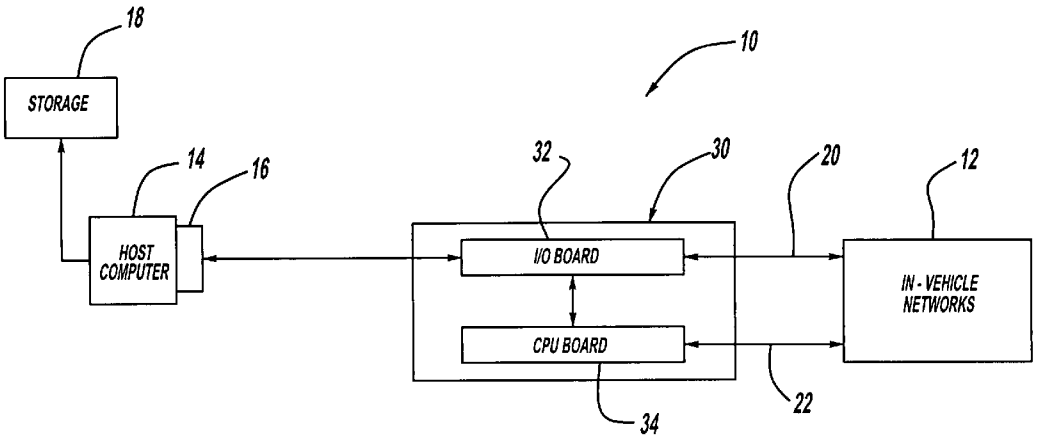
(57) **ABSTRACT**

A protocol adapter for transferring diagnostic messages between networks within a vehicle and a host computer. The protocol adapter operates as a voltage translator to support J1708 software. The protocol adapter also recognizes when the protocol adapter is connected to a host computer running the J1939 and/or J1708 protocols and automatically switches to that protocol.

16 Claims, 9 Drawing Sheets



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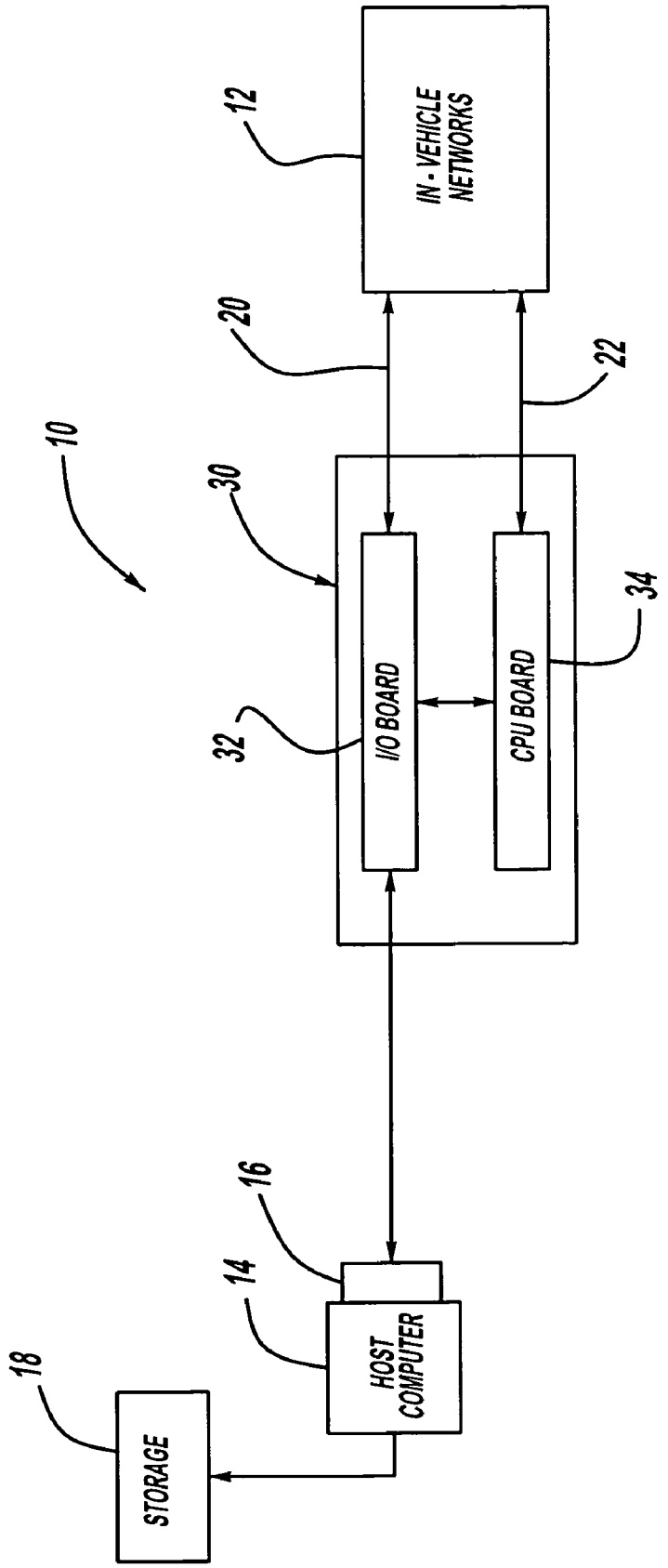

IN - VEHICLE NETWORKS
12
20
22
10
30
I/O BOARD
CPU BOARD
34
32
16
14
HOST COMPUTER
18
STORAGE

FIG - 1

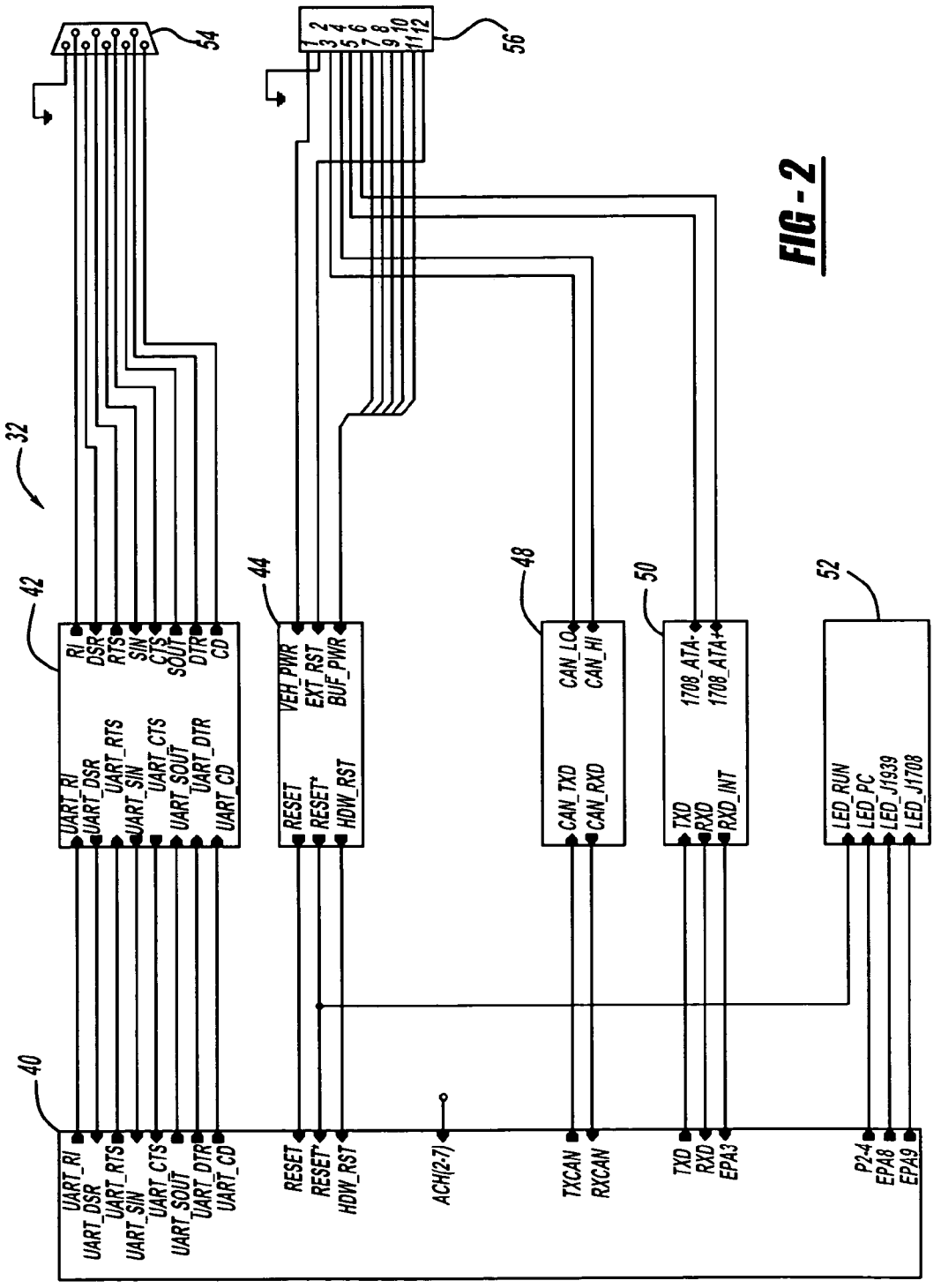

54
56
32
42
44
48
50
52
40
RI
DSR
RTS
SIN
CTS
SOUT
DTR
CD
UART_RI
UART_DSR
UART_RTS
UART_SIN
UART_CTS
UART_SOUT
UART_DTR
UART_CD
VEH_PWR
EXT_RST
BUF_PWR
RESET
RESET*
HDW_RST
CAN_LO
CAN_HI
CAN_TXD
CAN_RXD
1708_ATA-
1708_ATA+
TXD
RXD
RXD_INT
LED_RUN
LED_PC
LED_J1939
LED_J1708
ACH(2-7)
TXCAN
RXCAN
EPA3
P2.4
EPA8
EPA9

FIG - 2

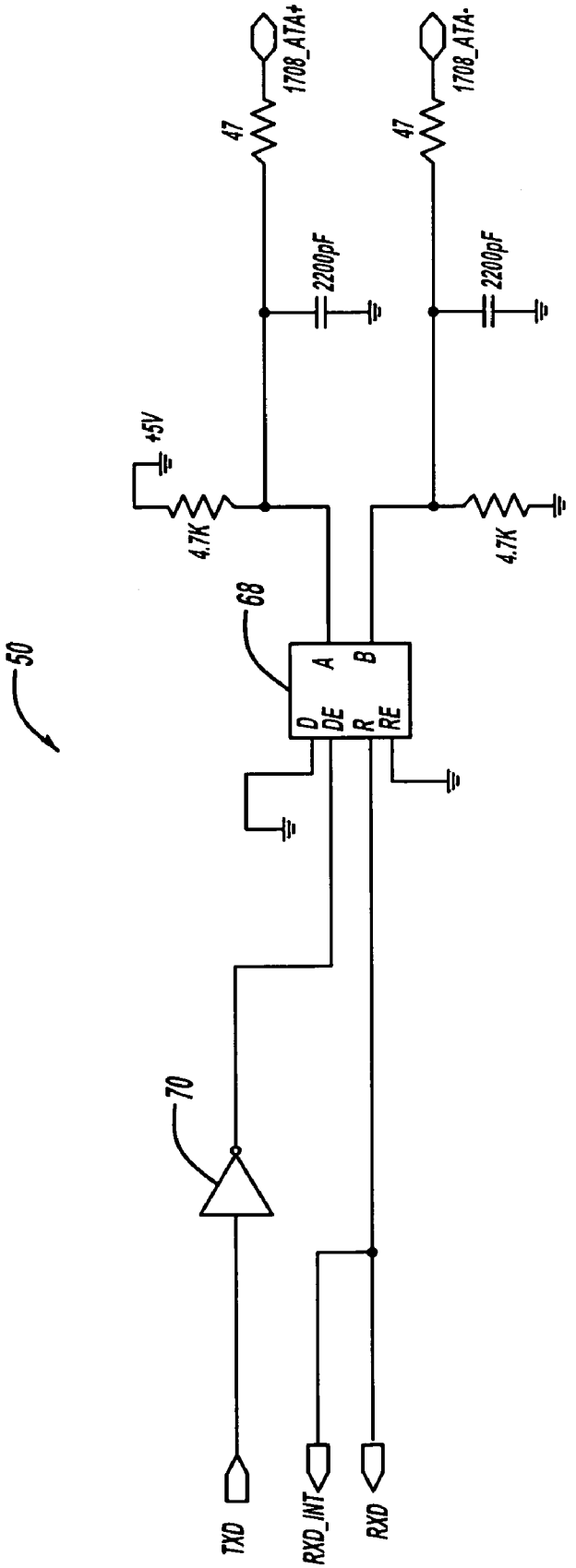

1708_ATA+
1708_ATA-
47
47
2200pF
2200pF
+5V
4.7K
4.7K
68
50
A
B
D
DE
R
RE
70
TXD
RXD_INT
RXD

FIG - 3

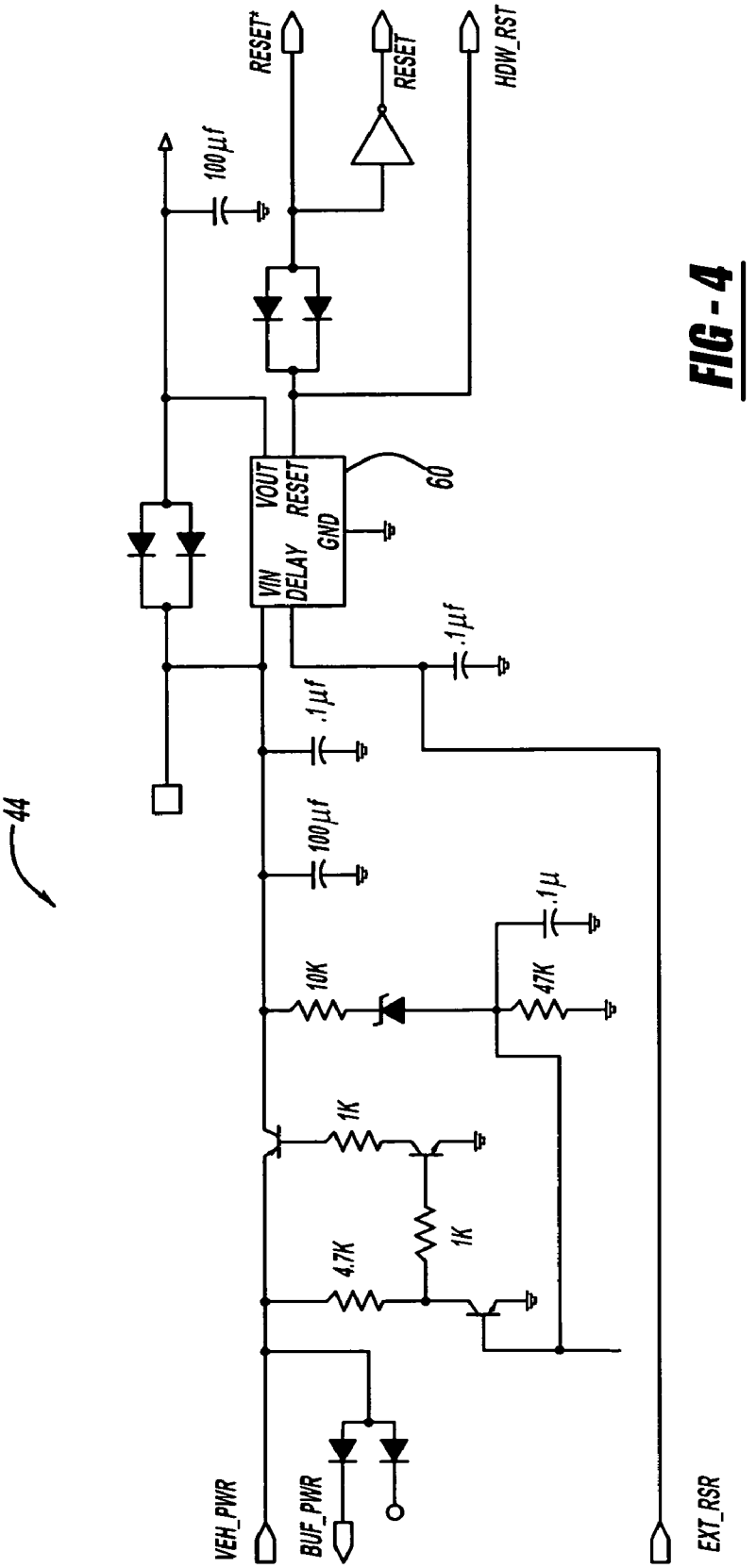

RESET*
RESET
HDW_RST
100µf
VOUT
RESET
GND
VIN
DELAY
60
.1µf
.1µf
100µf
.1µ
10K
47K
1K
1K
4.7K
44
VEH_PWR
BUF_PWR
EXT_RSR

FIG - 4

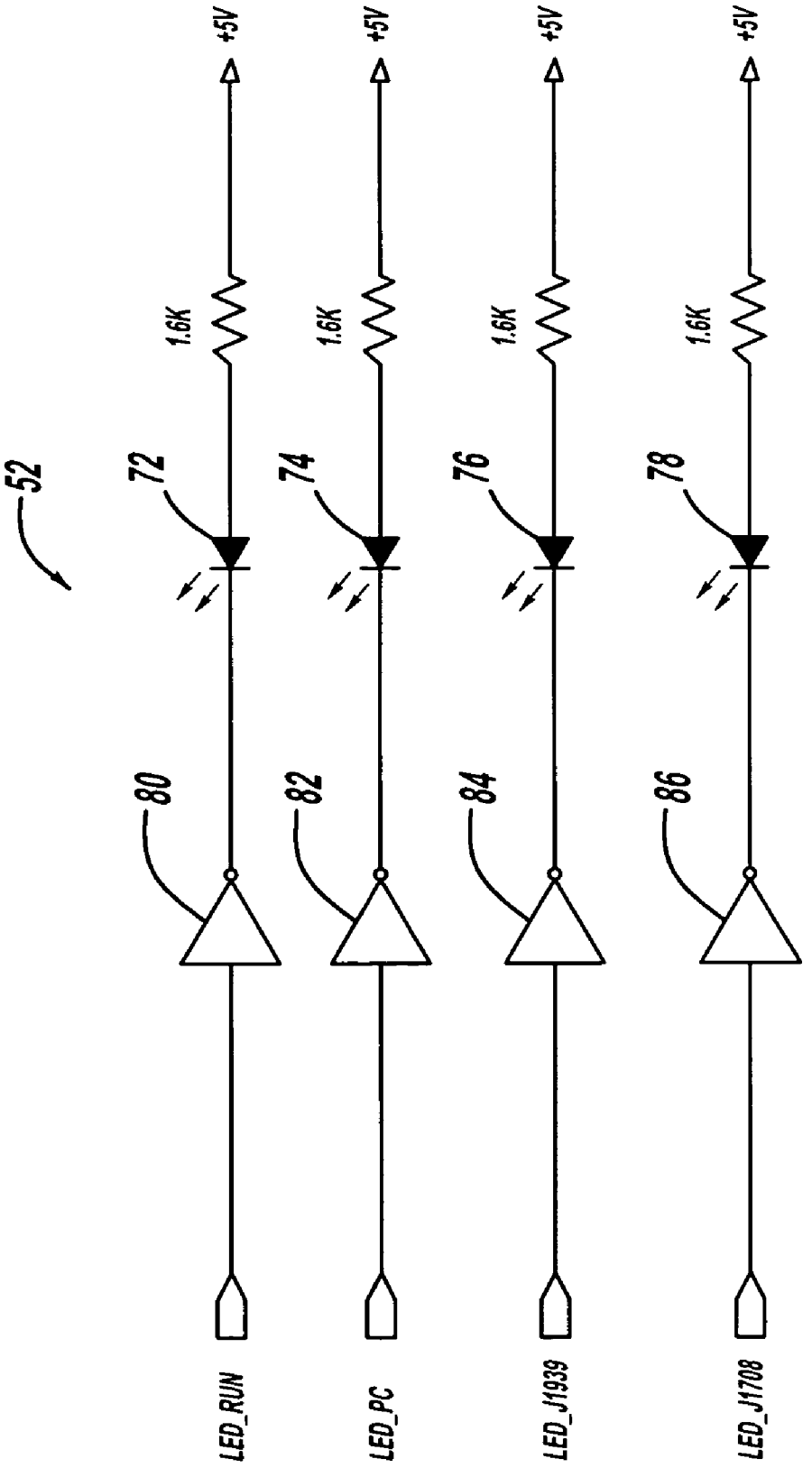
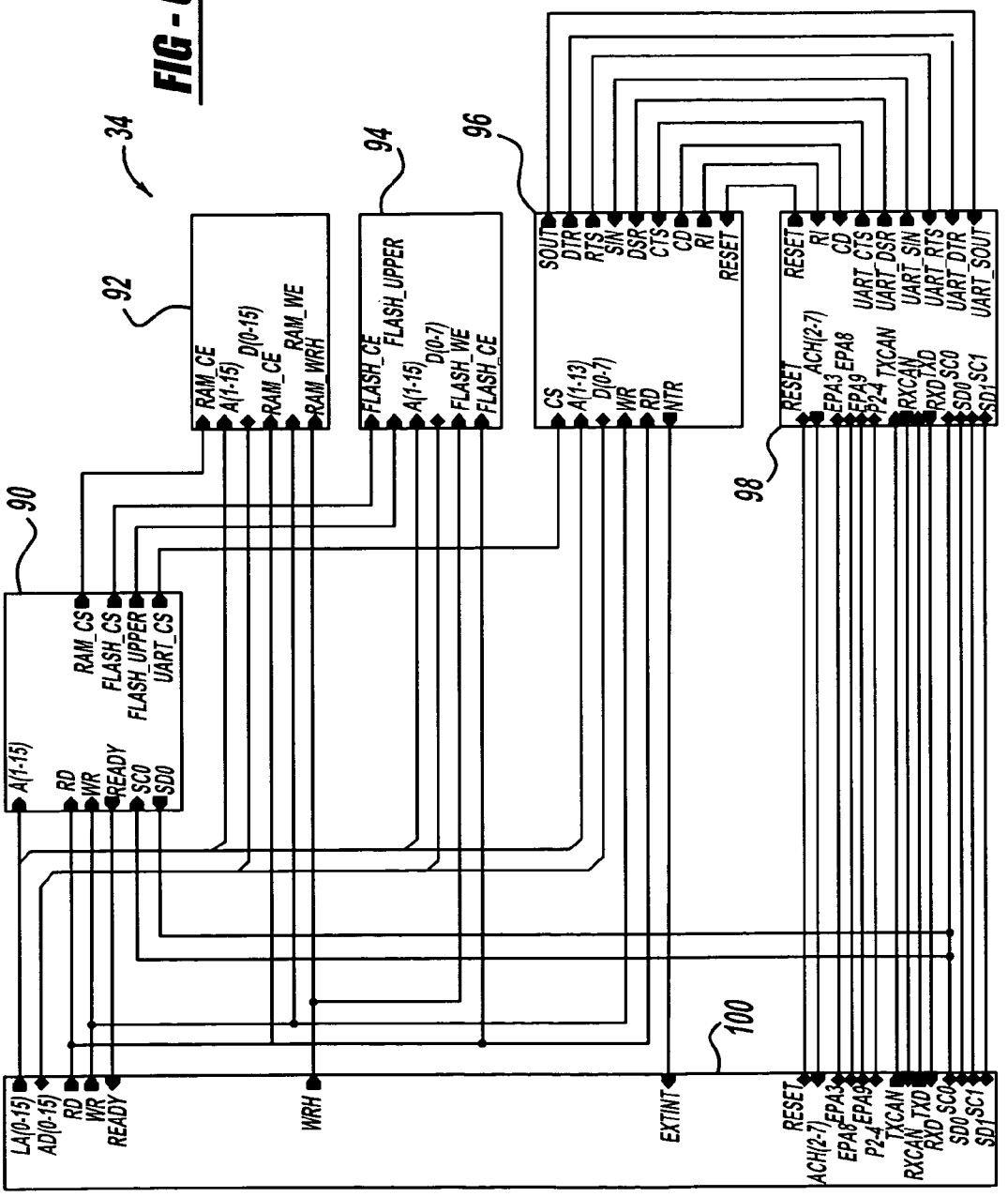

52
72
74
76
78
80
82
84
86
+5V
+5V
+5V
+5V
1.6K
1.6K
1.6K
1.6K
LED_RUN
LED_PC
LED_J1939
LED_J1708

FIG - 5

FIG - 6


34
92
94
96
98
90
100
RAM_CE
A(1-15)
D(0-15)
RAM_CE
RAM_WE
RAM_WRH
FLASH_CE
FLASH_UPPER
A(1-15)
D(0-7)
FLASH_WE
FLASH_CE
SOUT
DTR
RTS
SIN
DSR
CTS
CD
RI
RESET
CS
A(1-13)
D(0-7)
WR
RD
INTR
RESET
RI
CD
UART_CTS
UART_DSR
UART_SIN
UART_RTS
UART_DTR
UART_SOUT
RESET
ACH(2-7)
EPA3
EPA8
EPA9
P2-4
TXCAN
RXCAN
TXD
RXD
SCO
SDO
SC1
SD1
RAM_CS
FLASH_CS
FLASH_UPPER
UART_CS
A(1-15)
RD
WR
READY
SCO
SDO
LA(0-15)
AD(0-15)
RD
WR
READY
WRH
EXTINT
RESET
ACH(2-7)
EPA3
EPA8
EPA9
P2-4
TXCAN
RXCAN
TXD
RXD
SCO
SDO
SC1
SD1

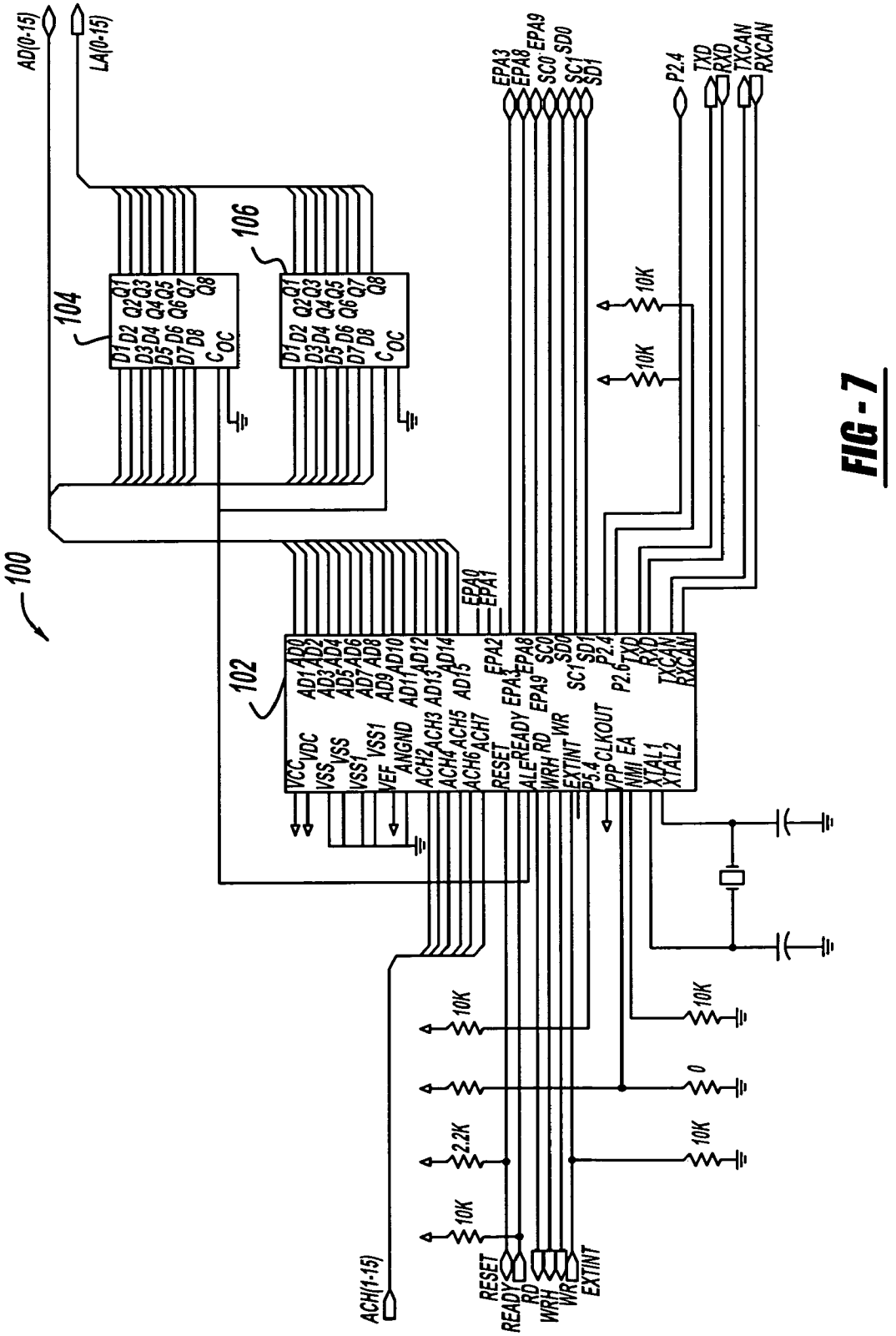

AD(0-15)
LA(0-15)
100
102
104
106
EPA3
EPA8
SC0
SD0
EPA9
SC1
SD1
P2.4
TXD
RXD
TXCAN
RXCAN
10K
10K
10K
0
10K
2.2K
10K
ACH(1-15)
RESET
READY
RD
WRH
WR
EXTINT

FIG - 7

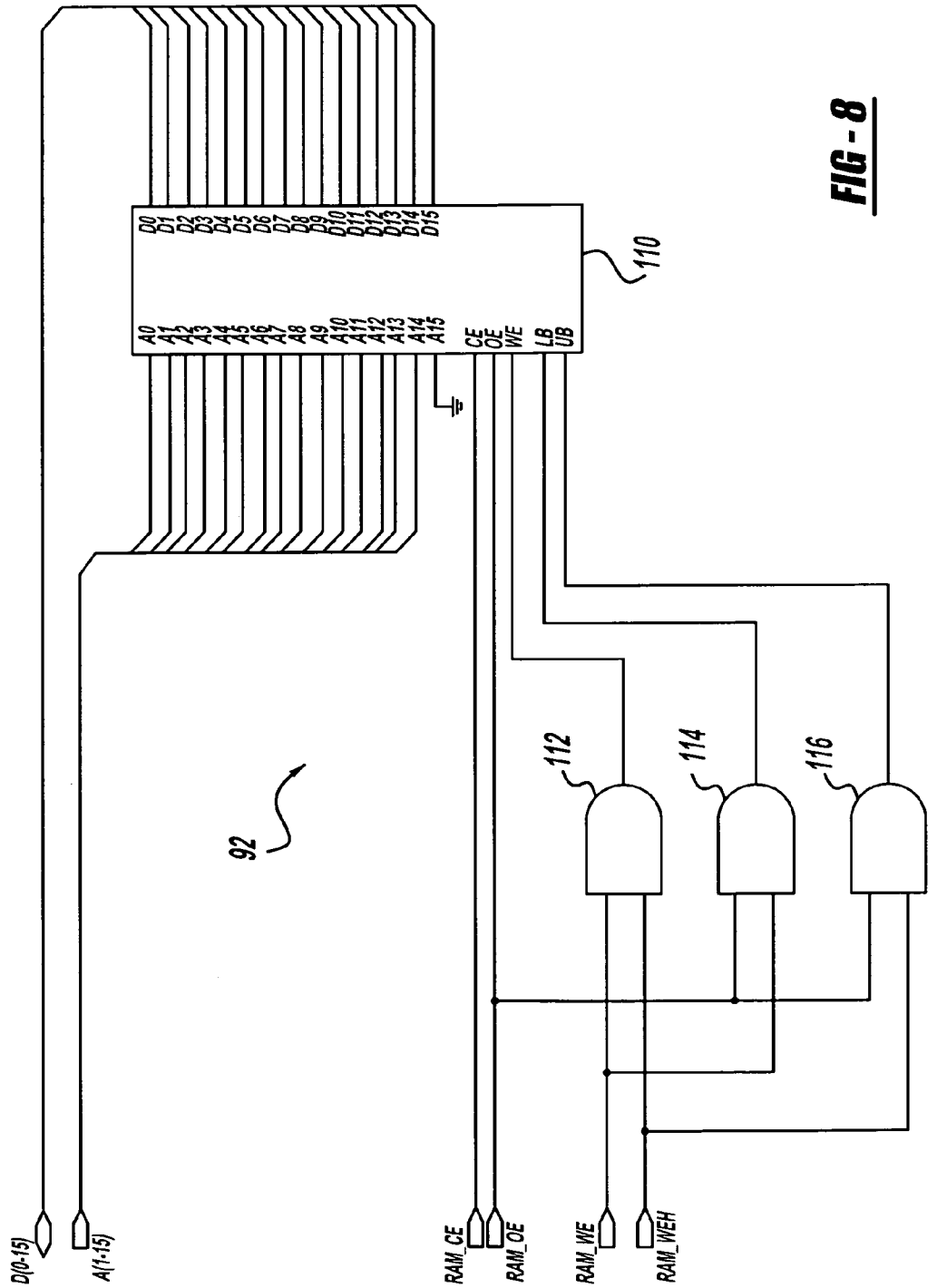

D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
CE
OE
WE
LB
UB
110
92
112
114
116
D(0-15)
A(1-15)
RAM_CE
RAM_OE
RAM_WE
RAM_WEH

FIG - 8

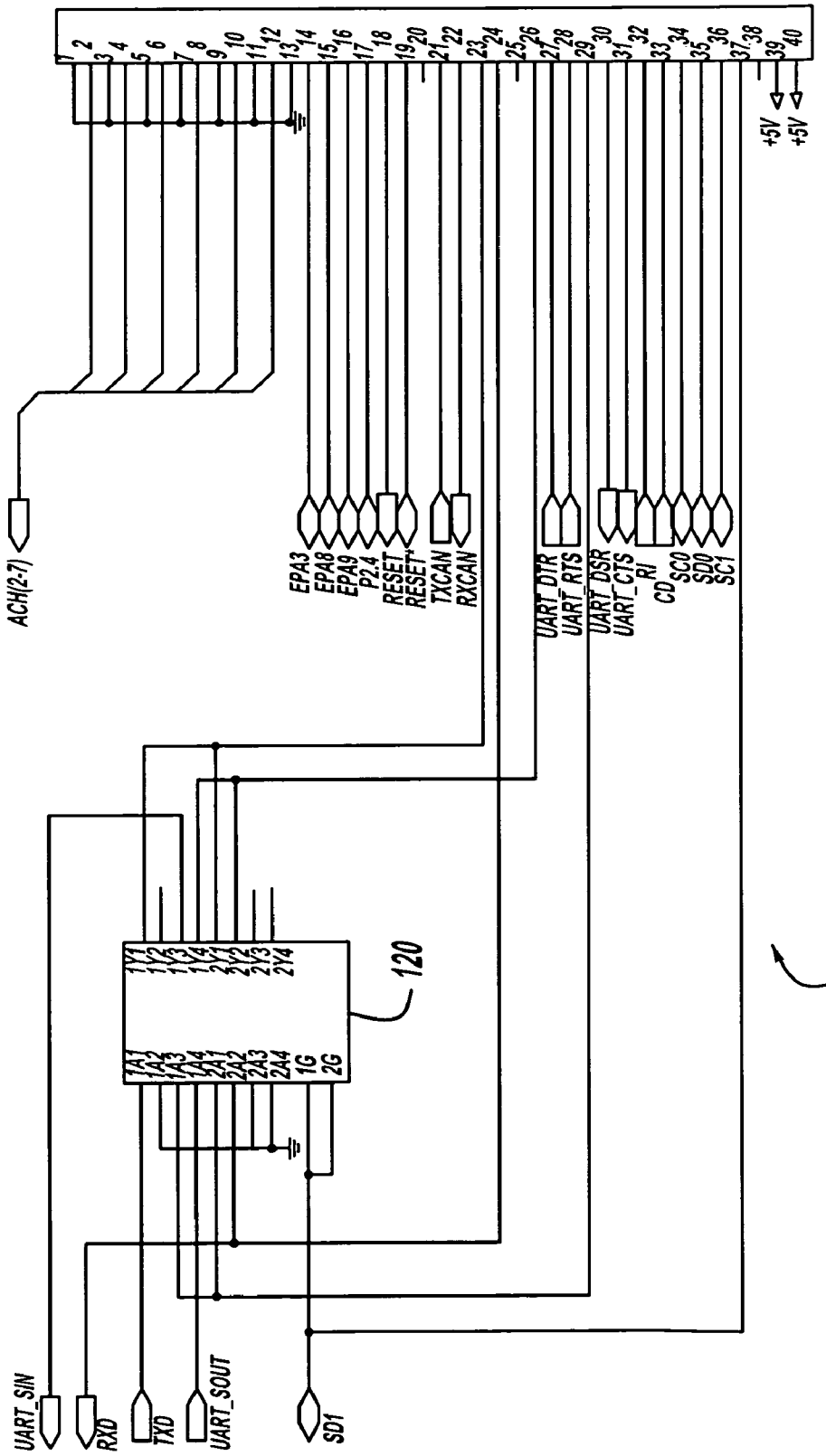

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40
+5V
+5V
ACH(2-7)
EPA3
EPA8
EPA9
P2.4
RESET_
RESET*
TXCAN
RXCAN
UART_DTR
UART_RTS
UART_DSR
UART_CTS
RI
CD
SC0
SD0
SC1
1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4
1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4 1G 2G
120
98
UART_SIN
RXD
TXD
UART_SOUT
SD1

FIG - 9

PROTOCOL ADAPTER FOR PASSING DIAGNOSTIC MESSAGES BETWEEN A HOST COMPUTER AND VEHICLE NETWORKS OPERATING IN J1939 OR J1708 PROTOCOL

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation Application of U.S. Ser. No. 12/799,739 filed Apr. 30, 2010, which is a continuation of U.S. Ser. No. 12/002,427 filed Dec. 17, 2007, which is a Divisional Application of U.S. application Ser. No. 10/888,432, filed Jul. 9, 2004, which is a Continuation-in-Part Application of U.S. application Ser. No. 09/532,718, filed Mar. 22, 2000, which claims the benefit of U.S. Provisional Patent Application Ser. No. 60/126,588, filed Mar. 26, 1999.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to a protocol adapter for passing diagnostic messages between networks within a vehicle and a host computer and, more particularly, to a protocol adapter for passing diagnostic messages between networks within a vehicle and a host computer, where the protocol adapter includes a pass-through mode of operation where the protocol adapter emulates legacy protocol adapters so that state of the art host computers can communicate with the vehicle networks using obsolete software.

2. Discussion of the Related Art

Vehicles employ various networks and systems for diagnostics, analysis and monitoring of vehicle systems. These various networks are generally selectively connectable to an external host computer so that the operation of the vehicle networks can be monitored by an external system. These vehicle systems and networks operate under various protocols, such as the J1708 and the J1939 protocols. Protocol adapters are known in the art that allow the host computer to communicate with the vehicle networks through the protocols.

One known type of protocol adapter for this purpose is the J1708 protocol adapter. The first generation of the J1708 protocol adapter used for diagnostic purposes included a voltage translator with a built-in-timer circuit that flagged the end of a message. This protocol adapter design worked well for J1708 protocols because it and the standard serial communication port of the host computer were based on universal asynchronous receive and transmit (UART) technology having different physical interfaces, i.e., different voltages. The timer circuit was needed to allow the host computer to recognize the end of message as defined by the J1708 protocol. Most host computers, however, did not have adequate resources to comply with the rigid timing requirements needed for end of message detection.

A second generation protocol for vehicle diagnostics purposes is the J1939 protocol. With the J1939 protocol, there was no longer a basic compatibility between the known host computer serial communication port and the J1939 protocol. It therefore became necessary for protocol adapters to use microprocessors in their diagnostic tools. These microprocessors would receive an entire message from one of the supported links, and do message validation, including end of message detection. The microprocessor would then forward the message on to the appropriate communication channel if it did not detect an error. This alleviated the need for the timer to detect the end of message, but also added an inherent delay between the vehicle data link and the host computer serial communication port.

The J1939 protocol required that software had to be matched to the diagnostic tool for which it was written. Obsolete software had to be paired with legacy hardware, and new software had to be paired with new hardware. This required that each diagnostic shop own and maintain several diagnostic tools. It would be desirable to have a protocol adapter that could operate as an old voltage translator to support obsolete software using the J1708 protocol, and recognize when the protocol adapter is connected to a host computer running new software to automatically switch to the J1939 protocol.

SUMMARY OF THE INVENTION

In accordance with the teachings of the present invention, a protocol adapter is disclosed for transferring diagnostic messages between networks within a vehicle and a host computer. The protocol adapter operates as a voltage translator to support J1708 software. The protocol adapter also recognizes when the protocol adapter is connected to a host computer running the J1939 and/or J1708 protocols and automatically switches to that protocol.

In one embodiment, the protocol adapter includes a control area network (CAN) transceiver circuit that provides an interface between the vehicle network and the host computer when the vehicle network is operating in a J1939 protocol and a J1708 transceiver that provides an interface between the vehicle network and the host computer when the vehicle network is operating in a J1708 protocol. The J1708 transceiver circuit includes a voltage translator for translating the voltage of the J1708 protocol signals. The protocol adapter further includes a static random access memory (RAM) circuit that provides temporary data storage and is connected to the CPU through data and address channels, a flash memory module that provides permanent storage of application data and loader application information, and a universal asynchronous receive and transmit (UART) circuit that provides communication of asynchronous data to and from the host computer.

Additional advantages and features of the present invention will become apparent from the following description and appended claims, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a protocol adapter system, according to an embodiment of the present invention, that transfers both J1708 and J1939 signals between a host computer and a vehicle network;

FIG. **2** is a schematic block diagram of an input/output (I/O) board in the protocol adapter shown in FIG. **1**;

FIG. **3** is a schematic diagram of a J1708 transceiver circuit in the I/O board shown in FIG. **2**;

FIG. **4** is a schematic diagram of a power supply regulator circuit in the I/O board shown in FIG. **2**;

FIG. **5** is a schematic diagram of an LED indicator circuit in the I/O board shown in FIG. **2**;

FIG. **6** is a schematic block diagram of a central processing unit (CPU) board in the protocol adapter shown in FIG. **1**;

FIG. **7** is a schematic diagram of the central processing unit in the CPU board shown in FIG. **6**;

FIG. **8** is a schematic diagram of a static memory module circuit in the CPU board shown in FIG. **6**; and

FIG. **9** is a schematic diagram of an I/O interface connector circuit in the CPU board shown in FIG. **6**.

DETAILED DESCRIPTION OF THE EMBODIMENTS

The following discussion of the embodiments of the invention directed to a protocol adapter for transferring both J1708 and J1939 protocol diagnostic messages between networks within a vehicle and a host computer is merely exemplary in nature, and is in no way intended to limit the invention or its applications or uses.

FIG. **1** is a block diagram of a system **10** for transferring diagnostic signals between vehicle networks **12** in a vehicle to an external host computer **14** through a protocol adapter **30**. Such diagnostic messages can be any signals for monitoring any suitable vehicle network within the vehicle for diagnostics and/or maintenance purposes, as would be well understood to those skilled in the art. The host computer **14** can be any host computer known in the art used for this purpose, including state of the art host computers and obsolete host computers. The host computer **14** includes an RS-232 I/O port **16** that provides an RS-232 interface to the host computer **14**. The RS-232 port **16** provides direct access to the J1708/RS-485 link. The signals received and analyzed by the host computer **14** can be stored in any suitable storage device **18**, such as a display or magnetic tape. The signals used by the vehicle networks **12** can be of any particular vehicle protocol, including the J1708 protocol provided on line **20** and the J1939 protocol provide on line **22**.

According to the invention, the protocol adapter **30** is compatible for both the J1708 protocol and the J1939 protocol. The protocol adapter **30** provides a "pass-through" interface so that various compliant applications from various developers can use any of the unique developer applications. This allows all compliant software applications and hardware interface adapters to be interchangeable. The protocol adapter **30** is capable of performing electronic control module (ECM) emulation, analysis of network message loading, simulation of message traffic loading of an in-vehicle network, inventory management, ECM code testing, a gateway between networks and vehicle maintenance status checks.

The protocol adapter **30** includes an I/O sub-assembly board **32** and a CPU sub-assembly board **34**, both of which will be described in detail below. When the vehicle networks **12** use the J1708 protocol, the protocol adapter **30** can operate in a pass-through mode where the J1708 signals on the line **20** are passed through a voltage translator directly to an RS-232 transceiver in the I/O board **32**. With the J1708 protocol, the protocol adapter **30** can also operate under the control of an embedded processor where the J1708 signals on the line **20** are passed through a voltage translator to be processed in the CPU board **34** and routed to an RS-232 transceiver (discussed below) in the I/O board **32**. If the vehicle networks **12** are using the newer J1939 protocol, the J1939 signals on the line **22** are processed in the CPU board **34** to provide the J1939 compatibility.

The I/O board **30** and the CPU board **34** use the following list of signals:

ACH[2.7]-inputs for the analog/digital converter
RESET*-active low signal issued to reset the processor
READY-signal used to lengthen memory cycles for slow memory
RD*-active low signal used for external memory reads
WRH*-active low signal used to designate high-byte writes

-continued

WR*-active low signal used for external writes
EXTINT-designates an external interrupt
AD[0.15]-address data lines to transfer between the processor and memory
LA[0.15]-latch address used to latch the desired memory bytes
EPA3-input/output for high speed capture/compare channels
EPA8-input/output for high speed capture/compare channels
EPA9-input/output for high speed capture/compare channels
SC0-clock pin for SSIO0
SD0-data pin for SSIO0
SC1-clock pin for SSIO0
SD1-data pin for SSIO0
P2.4-standared bi-directional ports for data transfer
TXD-used to transmit serial data
RXD-used to receive serial data
TXCAN-used to transmit CAN signal
RXCAN-used to receive CAN signal
A[9.15]-high level address for selecting large byte operations
HDW_RST*-active love hardware reset
FLASH_UPPER-FLASH upper byte
FLASH_CS*-active low enable FLASH chip select
RAM_CS*-active low enable RAM chip select
UART_CS*-active low enable UART chip select
D[0.15]-data signal used to transfer data bi-directionally between the processor and memory
A[1.15]-address signal used to select the desired memory allocation area
CE*_LOWER-active low chip enable for lower byte
DE*_LOWER-active low data enable for lower byte
WE*_LOWER-active low write enable for lower byte
CE*_UPPER-active low chip enable for upper byte
DE*_UPPER-active low data enable for upper byte
WE*_UPPER-active low write enable for upper byte
FLASH_UPPER-FLASH upper byte write enable
FLASH_CE*-active low FLASH chip enable
FLASH_DE*-active low FLASH data enable
FLASH_WE*-active low FLASH write enable
A[1.3]-address signal used to select the desired allocation area
D[0.7]-data signal used to transfer data bi-directionally between the processor and memory
CS*-active low chip select
RESET-signal used for reset
INTR-interrupt line to processor
SOUT-data out
DTR*-active low enable data terminal ready
RTS*-active low enable ready to send
MBAUD-used to set the processor in high speed mode. Unused in this application.
SIN-data in
DSR*-active low enable data set ready
CTS*-active low enable clear to send
EPA3-input/output for high speed for capture/compare channels
EPA8-input/output for high speed for capture/compare channels
EPA9-input/output for high speed for capture/compare channels
P2.4-PC LED control
UART_SOUT-UART data out
UART_DTR*-active low enable UART data terminal ready
UART_RTS*-active low enable UART ready to send
UART_SIN-UART data in
UART_DSR*-active low enable UART data set ready
UART_CTS*-active low enable UART clear to send

FIG. **2** is a schematic block diagram of the I/O board **32**. The (I/O) board **32** includes an external I/O interface circuit **40**, an RS-232 transceiver circuit **42**, a power supply regulator circuit **44**, a controller area network (CAN) transceiver circuit **48** for the J1939 protocol, a J1708 transceiver circuit **50** including a voltage translator, an LED indicator circuit **52** and input and output ports **54** and **56** interconnected as shown. The external I/O interface circuit **40** provides the interface connection between the various circuits in the I/O board **32** and the connections to the host computer **14** and the vehicle networks **12**. The RS-232 transceiver circuit **42** provides an RS-232 interface between the vehicle networks **12** and the host computer **14**.

The CAN transceiver circuit **48** provides a CAN interface between the vehicle networks **12** and the host computer **14**

when the vehicle networks **12** are operating in the J1939 protocol. In one embodiment, the CAN transceiver is the model P82C251T, well known to those skilled in the art. The J1708 transceiver circuit **50** provides the J1708 protocol interface between the vehicle networks **12** and the host computer **14**. FIG. **3** is a schematic diagram of the J1708 transceiver circuit **50** and includes a voltage translator **68** and an input buffer **70** electrically interconnected, as shown. In one embodiment, the voltage translator **68** is the model SN75176, well known to those skilled in the art.

Both the transceiver circuits **48** and **50** include transmit mailboxes for transmitting J1708 and J1939 messages to the networks **12** and receive mailboxes for receiving J1708 and J1939 messages from the networks **12**. The protocol adapter **30** allows the user to customize each transmitted message. The J1708 or J1939 message to be transmitted may include the relative time to the adapter timer, when the message transmission is to begin, the number of times the message is to be sent, the desired time interval between transmissions, the ID and data to be sent, the conditions for a call back announcing a successful transmission, the number of times the message should be sent before auto-deletion occurs, and whether to enable a call back announcing the time of message deletion. The J1708 or J1939 message received may include which protocol to scan, which bits should be masked by hardware-level filtering, which bits should be matched by hardware-level filtering, what information, such as mailbox number, time stamp, identifier, length of data, etc., should be sent to the host immediately upon receipt, and how the application will be notified when a message is received, such as transparent update, receive call back, polling, etc.

FIG. **4** is a schematic diagram of the power supply regulator circuit **44** and includes a voltage regulator **60** interconnected with other circuit elements, as shown. The power supply regulator circuit **44** converts a vehicle battery voltage to a regulated 5V DC for operation of the adapter **30**.

FIG. **5** is a schematic diagram of the LED circuit **52**. The LED circuit **52** includes four LED control lines coupled to four LEDs **72**, **74**, **76** and **78** through input buffers **80**, **82**, **84** and **86**, respectively. In this embodiment, the LED **72** indicates that the protocol adapter **30** is being powered, the LED **74** indicates a link to the RS-232 port **16** of the host computer **14**, the LED **76** indicates that the protocol adapter **30** is operating in the J1939 protocol and the LED **78** indicates that the protocol adapter **30** is operating in the J1708 protocol.

FIG. **6** is a schematic block diagram of the CPU board **34**. The CPU board **34** includes a CPU **100**, a device decoder circuit **90**, a static RAM circuit **92**, a flash memory module **94**, a UART circuit **96** and a CPU I/O interface circuit **98** electrically interconnected as shown. The flash memory module **94** is used for program storage. The module **94** is responsible for the permanent storage of the application data and loader application information. The module **94** allows the protocol adapter **30** to be updated with new firmware in the field. The uploaded firmware is stored in the RAM circuit **92**.

The UART circuit **96** is used for communication of asynchronous data to and from the programmable controller **14**. The UART circuit **96** is used to convert parallel data from the CPU **100** to serial data to the host computer **14**, and vice versa.

FIG. **7** is a schematic diagram of the CPU **100**, and includes a microprocessor **102** and two input/output chips **104** and **106** electrically coupled as shown. In this embodiment, the microprocessor **102** is the model 87C196CA and the chips **104** and **106** are the model 74HC573. In the pass through mode, the microprocessor **102** delivers data directly to the J1708 transceiver circuit **50** to the RS-232 transceiver circuit **42**, and monitors the data so as to provide the J1708 defined timing signals on any or all of the RS-232 hardware handshake signals.

FIG. **8** is a schematic diagram of the static RAM circuit **92**, and includes a memory chip **110** and AND gates **112**, **114** and **116** electrically interconnected as shown. In one embodiment, the memory chip **110** is the model TC551664BJ-20, well known to those skilled in the art. The memory chip **110** is used for temporary data storage and is connected to the CPU **100** through the data and address channels. Once a memory allocation area is specified through the address channel, data can be read or written through the data channel. Data signals D(**0-15**) are used to transfer data bi-directionally between the CPU **100** and the memory chip **110**. Address signals A(**1-15**) are used to select the desired memory allocation area in the memory chip **110**.

The static RAM circuit **92** provides space reserved in the adapter's memory for the temporary storage of data for the transmit and receive mailboxes. The static RAM circuit **92** provides flexibility for transmitting and receiving messages, regardless of the J1708 or J1939 vehicle protocol, by providing a temporary message storage location, redirection of mailbox data, storage for oversized messages, such as J1939 transport protocol messages, and the concatenation of small messages.

Sometimes both the J1708 and the J1939 protocols transmit oversized messages. A normal J1708 message may be up to 21 bytes long. However, special modes may utilize longer messages. The protocol adapter **30** accommodates these oversized messages by putting the J1708 mailbox into extended mode and attaching it to a location in the static RAM circuit **92**. The J1939 transport layer also makes use of the RAM circuit **92** to ensure that transport timing requirements are met. The storing of multiple messages in the static RAM circuit **92** reduces multiple reads and writes to the adapter hardware. The concatenation of these short messages reduces the overhead on the serial port. The static RAM circuit **92** allows users to replace legacy hardware with an interface that can support existing software. Consequently, users can replace legacy hardware with the protocol adapter **30** and maintain compatibility with their original software.

FIG. **9** is a schematic diagram of the CPU I/O interface circuit **98**, and includes an interface chip **120**. In one embodiment, the interface chip **120** is the model 74HC241. The interface circuit **98** provides interfacing between the CPU **100** and the I/O board **32**.

The foregoing discussion discloses and describes merely exemplary embodiments of the present invention. One skilled in the art will readily recognize from such discussion and from the accompanying drawings and claims that various changes, modifications and variations can be made therein without departing from the spirit and scope of the invention as defined in the following claims.

What is claimed is:

1. A protocol adapter for transferring diagnostic messages between a vehicle network in a vehicle and an external host computer, said adapter comprising:

a plurality of transceiver circuits for providing an interface between the vehicle network and the host computer when the vehicle network is operating in one of a plurality of protocols;

wherein the adapter automatically switches to one or more of the plurality of protocols the host computer is using; and further comprising a central processing unit (CPU), said CPU controlling the operation of the plurality of transceiver circuits to automatically switch between the

plurality of transceiver circuits, depending on which of the plurality of protocols the host computer is using.

2. The protocol adapter according to claim **1** one of said plurality of transceiver circuits further comprising an RS-232 transceiver, said RS-232 transceiver circuit providing an interface to an RS-232 port on the host computer.

3. The protocol adapter according to claim **1**, further comprising a device decoder, said device decoder decoding input signals sent to the CPU.

4. The protocol adapter according to claim **1**, further comprising a static random access memory (RAM) circuit, said RAM circuit including a RAM that provides temporary data storage and is connected to the CPU through data and address channels.

5. The protocol adapter according to claim **4** wherein the RAM circuit further provides redirection of mailbox data, storage for oversized messages and the concatenation of small messages.

6. The protocol adapter according to claim **1**, further comprising a flash memory module, said flash memory module providing permanent storage of application data and loader application information.

7. The protocol adapter according to claim **1**, further comprising a universal asynchronous receive and transmit (UART) circuit, said UART circuit providing communication of asynchronous data to and from the host computer.

8. The protocol adapter according to claim **1**, further comprising a CPU I/O interface circuit, said CPU I/O interface circuit providing an interface between the CPU and the transceiver circuits.

9. A protocol adapter for transferring diagnostic messages between a vehicle network in a vehicle and an external host computer, said adapter comprising:

a plurality of transceiver circuits for providing an interface between the vehicle network and the host computer when the vehicle network is operating in one of a plurality of protocols;

a central processing unit (CPU), said CPU controlling the operation of the plurality of transceiver circuits to automatically switch between the plurality of transceiver circuits, depending on which of the plurality of protocols the host computer is using; and

a voltage translator for translating the voltage of one or more of said plurality of protocols, said voltage translator being part of one of said plurality of transceiver circuits.

10. The protocol adapter according to claim **9**, one of said plurality of transceiver circuits further comprising an RS-232 transceiver, said RS-232 transceiver circuit providing an interface to an RS-232 port on the host computer.

11. The protocol adapter according to claim **9**, further comprising a static random access memory (RAM) circuit, said RAM circuit including a RAM that provides temporary data storage and is connected to said CPU through data and address channels.

12. The protocol adapter according to claim **11** wherein the RAM circuit further provides redirection of mailbox data, storage for oversized messages and the concatenation of small messages.

13. The protocol adapter according to claim **9** further comprising a flash memory module, said flash memory module providing permanent storage of application data and loader application information.

14. The protocol adapter according to claim **9** further comprising a universal asynchronous receive and transmit (UART) circuit, said UART circuit providing communication of asynchronous data to and from the host computer.

15. The protocol adapter according to claim **9**, further comprising a CPU I/O interface circuit, said CPU I/O interface circuit providing an interface between said CPU and the transceiver circuits.

16. The protocol adapter according to claim **9**, one of said plurality of transceiver circuits further comprising a J1708 transceiver circuit, said J1708 transceiver circuit providing an interface between the vehicle network and the host computer when the vehicle network is operating in a J1708 protocol and the protocol adapter is operating in a pass-through mode, said J1708 transceiver circuit including the voltage translator for translating the voltage of the J1708 protocol signals.

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